Precision Materials to Meet Scaling Challenges Beyond 14nm

Semicon 2013

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SSG Transistor Technology Group

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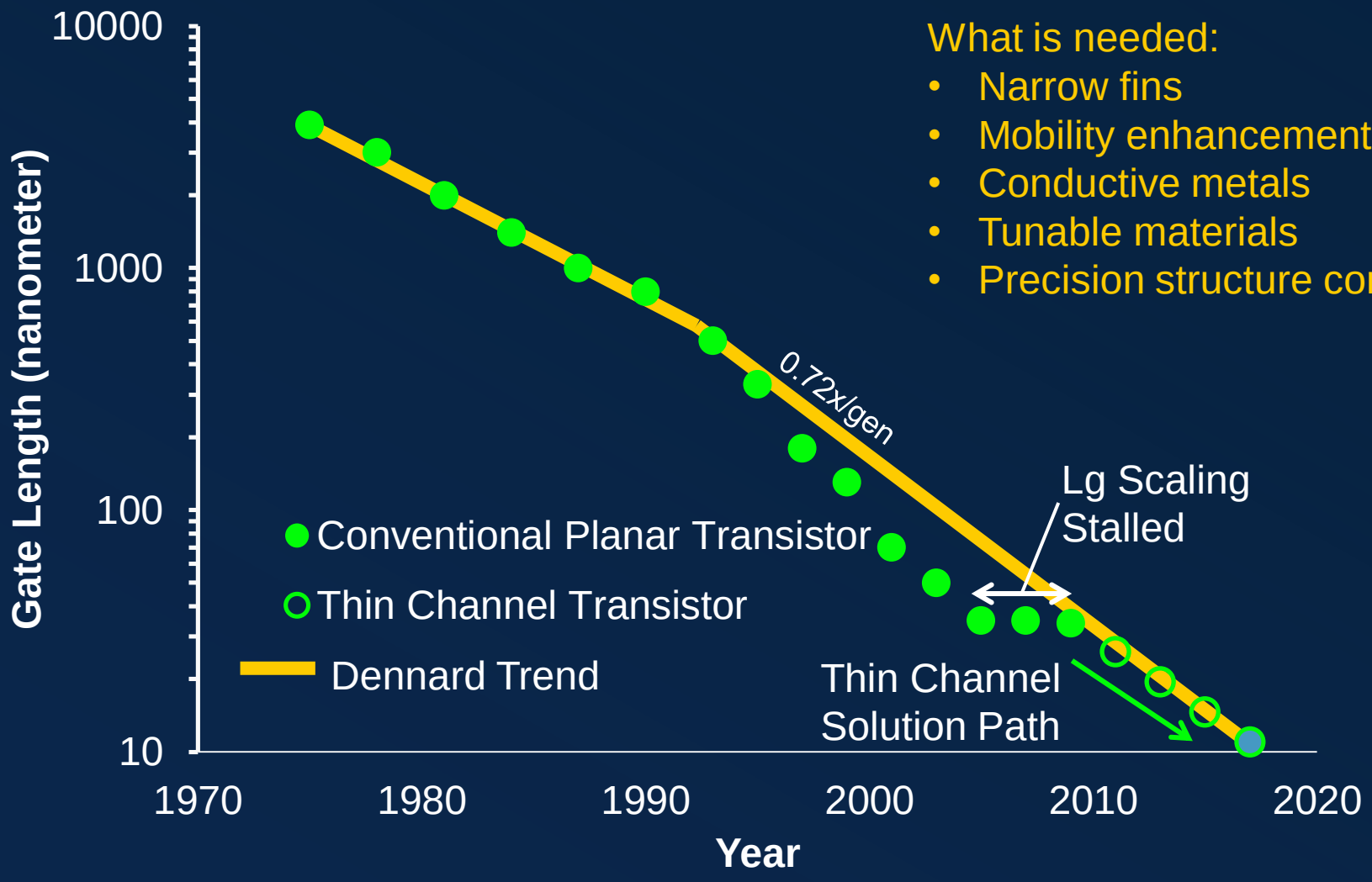
Continue The Lg Scaling Path



What is needed:

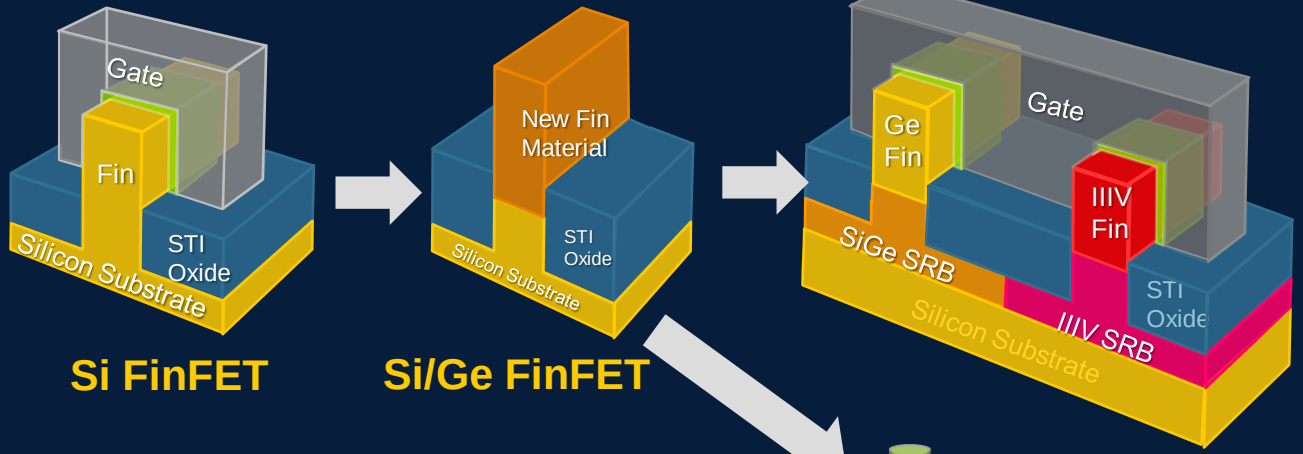
- Narrow fins
- Mobility enhancement
- Conductive metals
- Tunable materials
- Precision structure control

Transistor Pathway

n22, n14

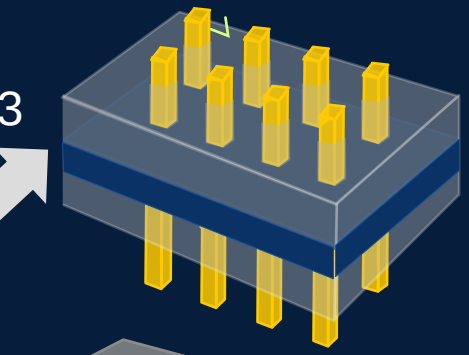
n10, n7

n5, n3



Si FinFET

Si/Ge FinFET



Si/Ge Gate All Around (GAA)
Vertical or Horizontal

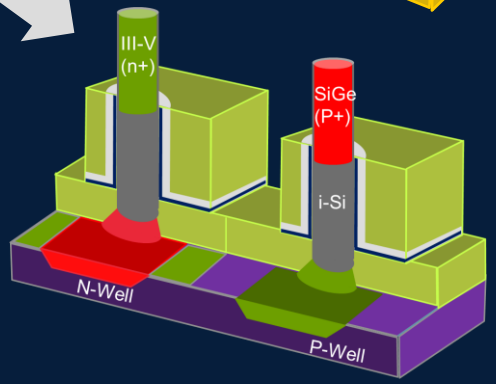
Improved electrostatics

- Precision etch and CMP
- Scaled metals
- High Aspect Ratio ALD

III-V FinFET

Improved mobility

- Epi structure
- III-V gate interface
- New material CMP



Vertical TFET

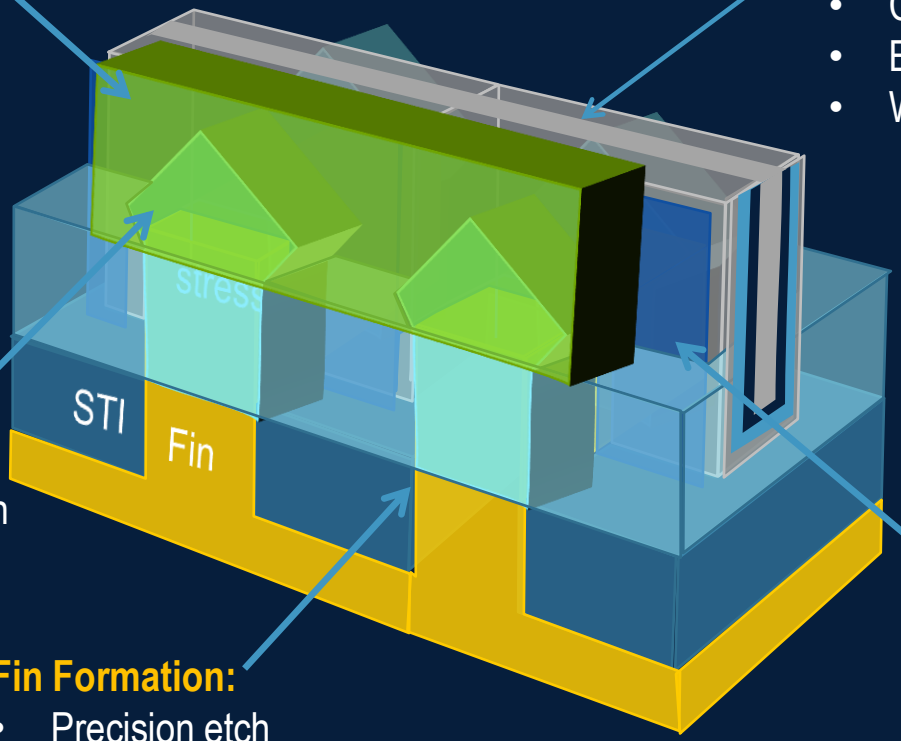
Improved SS

- Epi structure
- Multi-pass CMP
- Precision etch & CMP

FinFET Structure Control

Gate Structure Control
- Precision CMP
- Selective materials

Scaled High-K / Metal Gate
- Scaled EOT
- Conductive fill
- Band Edge workfunction materials
- WF modification for multi-Vt



Low Rc contact
- Integrated silicide preclean
- Interface modification

Parasitic Reduction
- Low K spacer and etch stop
- Dielectric mold for stressor

Fin Formation:
- Precision etch
- Scaled fin profile and STI fill
- Precision recess control
- High mobility channel materials

Precise control of materials is needed to deliver the required structure

Precision Materials Engineering

Optimizing the material to tune in the required property

Examples from Literature

Source	Modification	Effect
J Buhler 1997	Phos implant into SiO2	HF etch rate ↑
G Tam 1989	H Implant into SiN	HF etch rate ↑ Phosphoric ER↓
Hochbauer 2002	H implant into Si	Strain fracture
J Brugger 1997	Ge ion beam into Si	KOH etch rate ↓

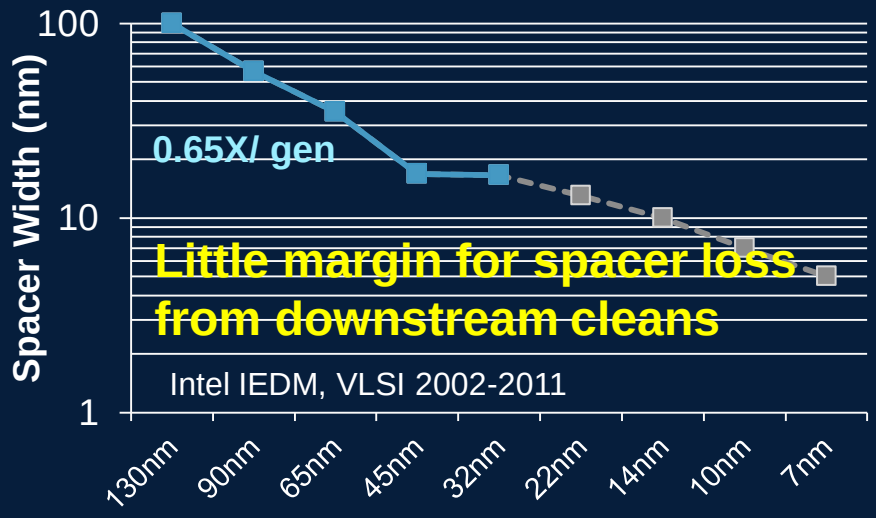
PME Opportunities

Implant + Etch ⇒ better control

Implant + Anneal ⇒ material property

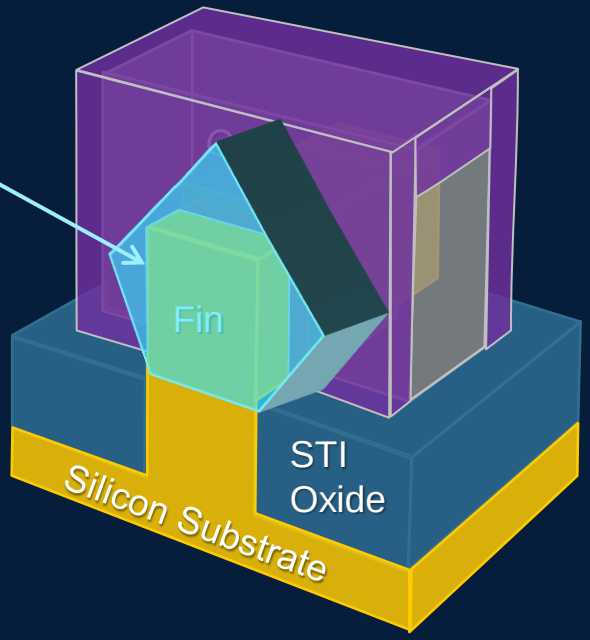
Epi, CMP, Etch, ALD ⇒ precise control

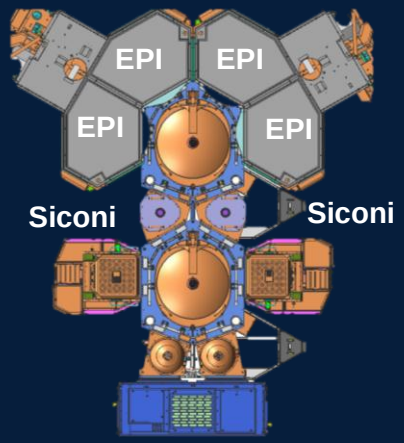
Example Challenge: Spacer Width Scaling

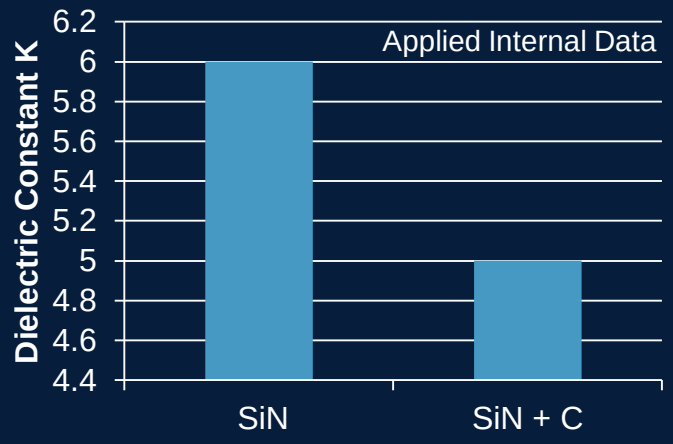


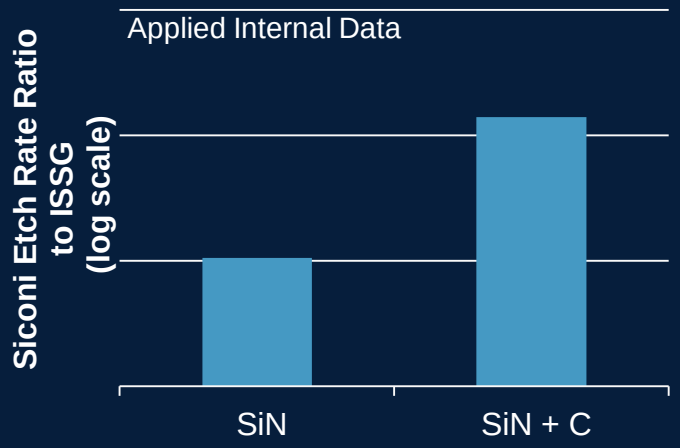
PME: C Addition to Spacer Improves K and Etch Ratio

Pre-epi clean exposes spacer nitride to oxide removal etch





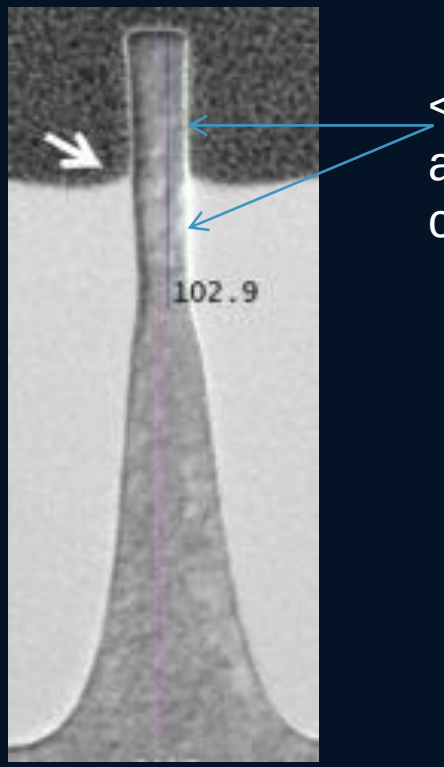




Siconi Fin Recess

Si etch selectivity 100:1

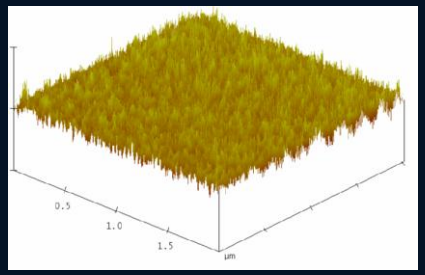
Smooth silicon and oxide surface



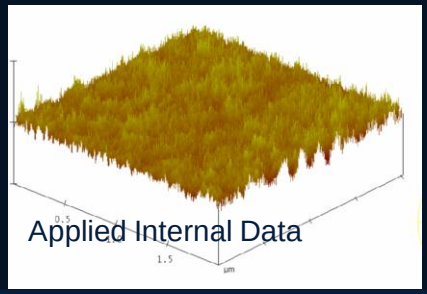
<1° sidewall angle change

Source: IMEC/Applied Materials

Reference No Siconi
RMS = 0.37 nm



After Siconi
RMS = 0.34 nm

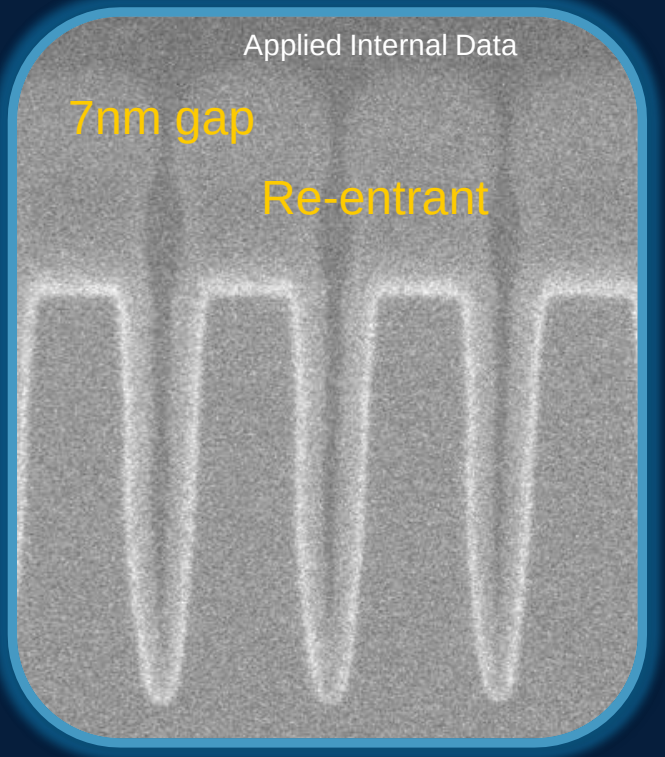


Applied Internal Data

APPLIED MATERIALS®

Flowable CVD Extendable Gap Fill Capability

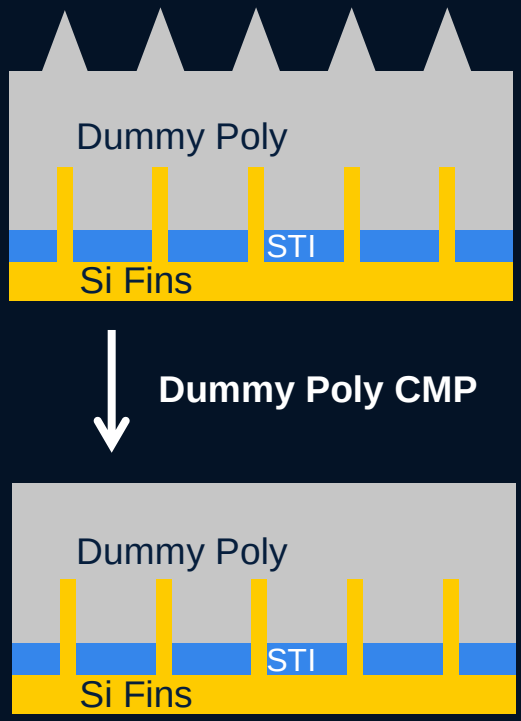
Reentrant Structure Fill



Excellent dielectric gapfill with low thermal budget for FinFET applications

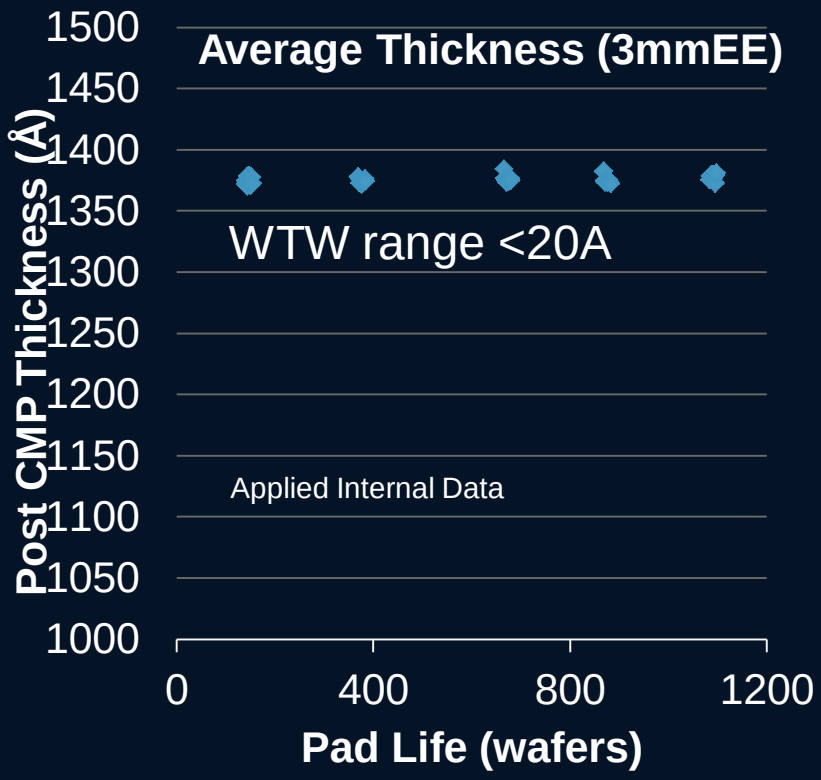
Fin Dummy Gate CMP Challenge: Stop in Film

Eliminate Dummy Gate Topology



In-Situ Optical Endpoint Allows Stop in Film

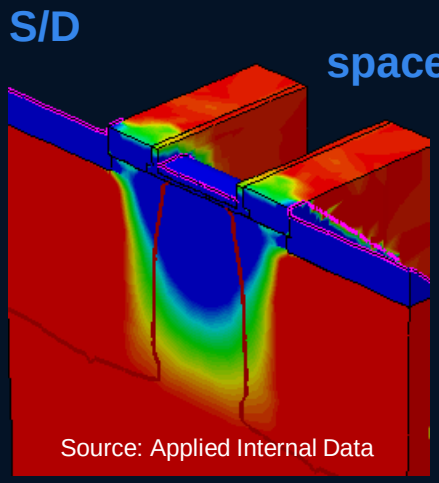
In Situ Process Control on Poly CMP



Angstrom-level thickness control

FinFET Mobility Enhancement

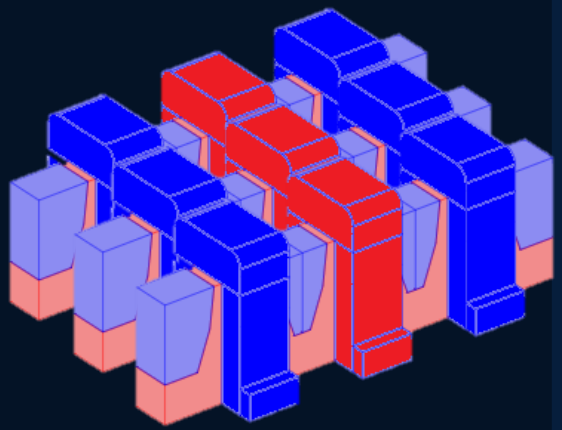
Replacement Stressor



Replacement vs. Wrap
>50% vs. 10%

Structure Design

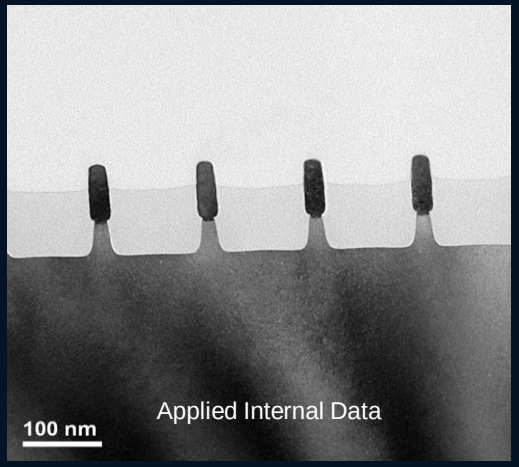
Replacement source/drain with non-merged Epi



Source: Penn State University

Highest-strain Si Option
70% of planar strain

High Mobility Channel



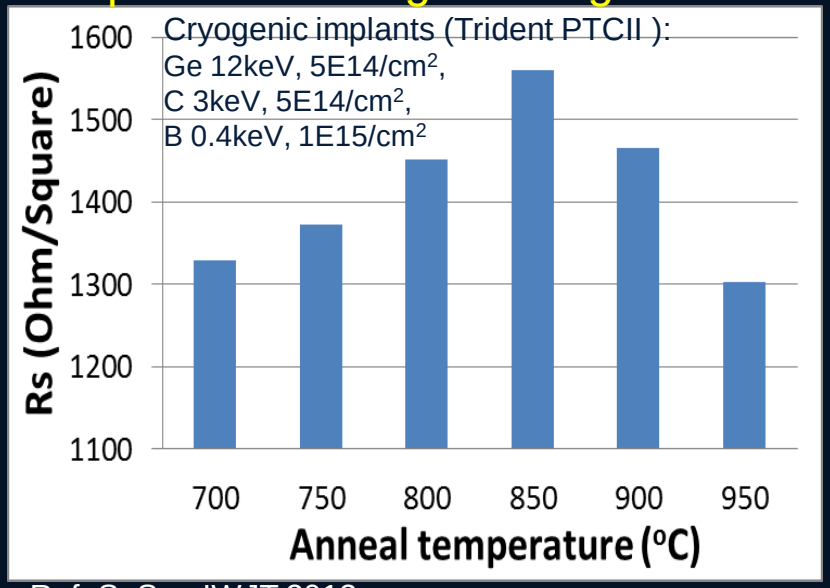
Germanium Fin

Precision Anneal by Millisecond Laser Treatment

Avoid Excess Dwell Temperature

Solution: low stabilization and fast cool down

Dopant Clustering with High Preheat

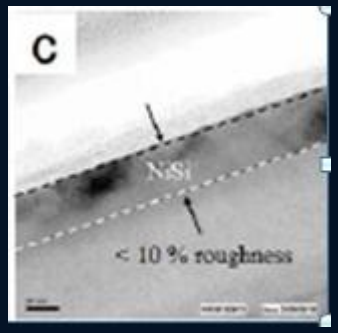


Ref: S. Sun IWJT 2013

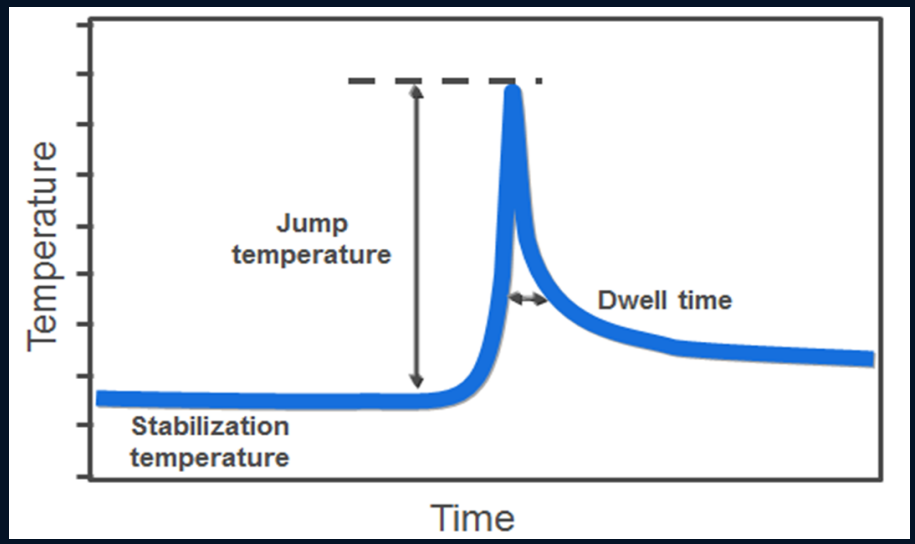
NiSi Conversion interface improvement

Soak

Chen, IEEE-RTP2009 Conference: Advances on 32nm NiPt Silicide



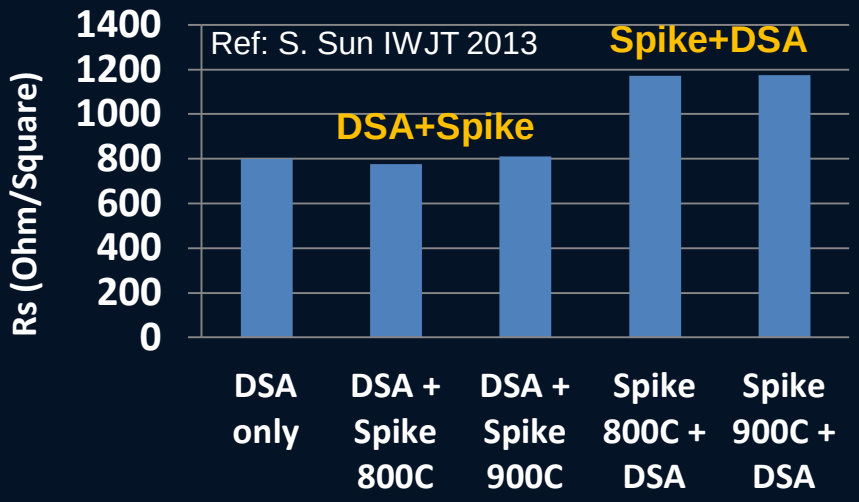
Laser



Architecture requirement is low stabilization temperature

SDE Extension Control By DSA Laser Anneal

Millisecond Anneal & Low chuck temp

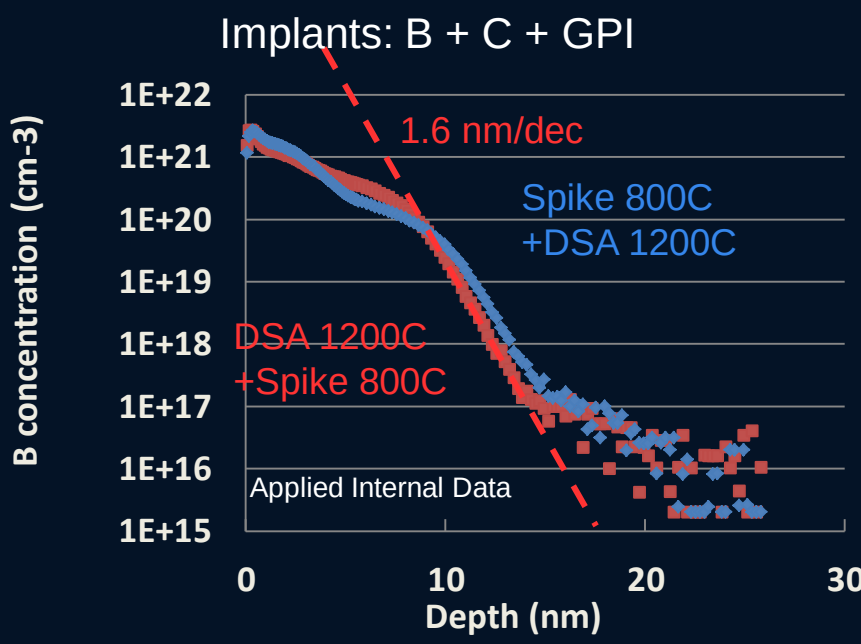


DSA laser / Spike sequence simulates higher stabilization temperature

Initial 800-900C exposure leads to Boron-Interstitial Cluster formation

Low stabilization T+ laser anneal gives best activation

Low chuck temp & Fast cool down



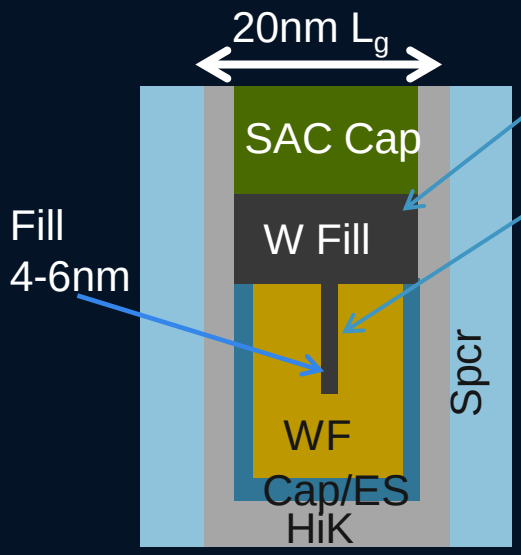
Less diffusion

Better activation and sharper junction

RMG Metal Gate Strategies

Double Etchback

- Tunable, band-edge
- Workfunction recess
- Conductive W fill



Complex Integration

Solutions

Tungsten Fill
Low R_s

Trident Implant
Adjust Workfunction

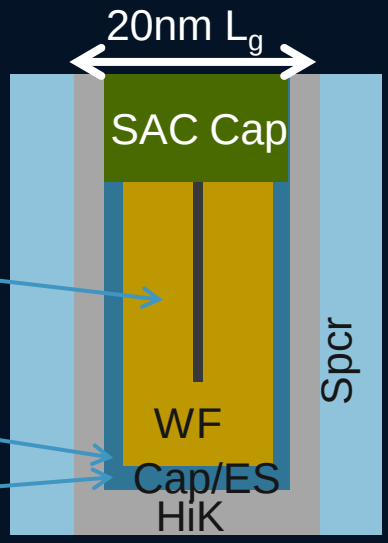
ALD WF
Tunable Workfunction

ALD TaN etch stop
multiple WF metal etches

ALD TiN / TiSiN
Improved Al barrier

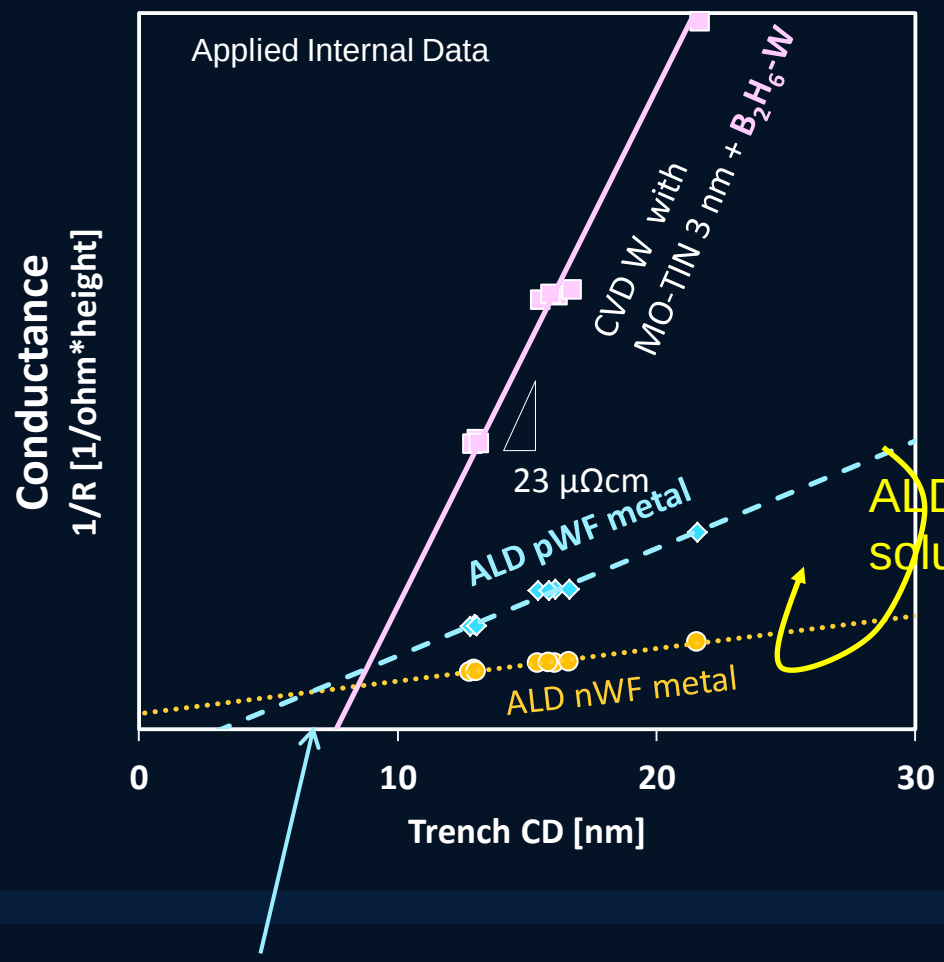
Workfunction as Fill

- Conductive WF
- W fill seals seam
- Longer L_g uses W fill

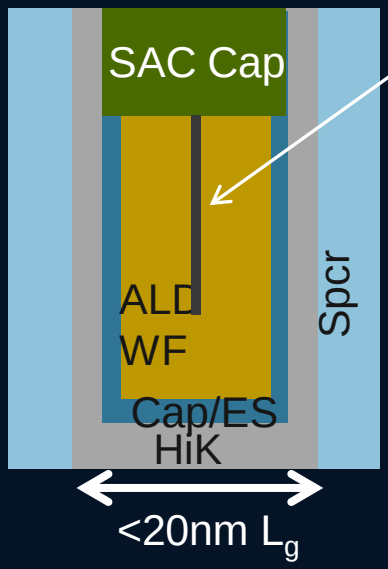


Enabled by low R_s ALD WF Materials

Metal Fill Scaling



Gap Fill Extendibility



Fill <6nm: Poor low L_g conductance

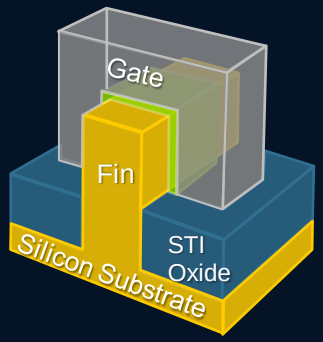
ALD WF fill reduces materials complexity

Below 10nm CD, thick ALD workfunction has best conductance

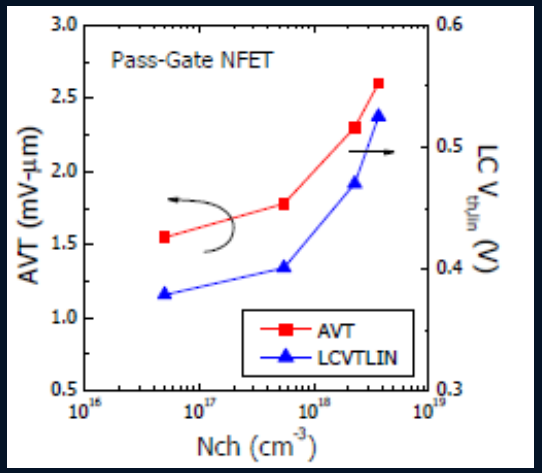
Metal Gate Workfunction Tuning

Objective:
reduce channel doping fluctuation

Solutions:
WF metal composition tuning

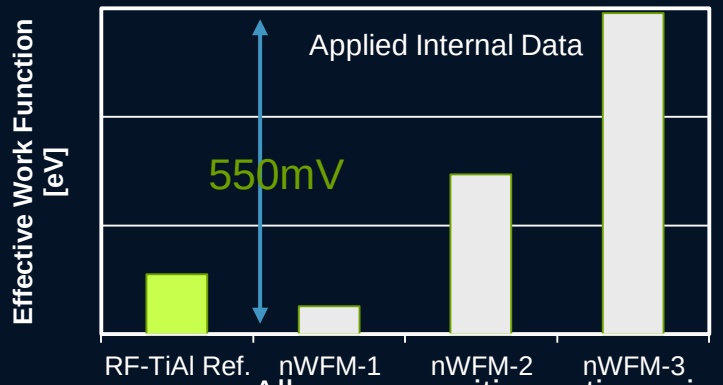


Channel doping increases Vt fluctuation:



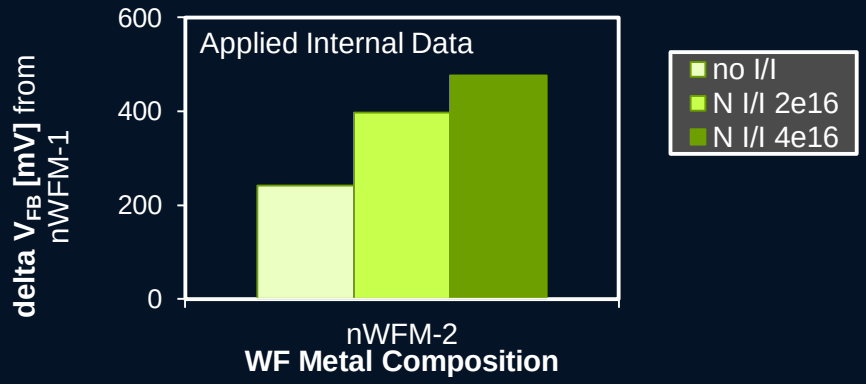
Ref: IBM CH Lin
VLSI 2012

Tuning of WF metal by deposition



Alloy composition ratio varied

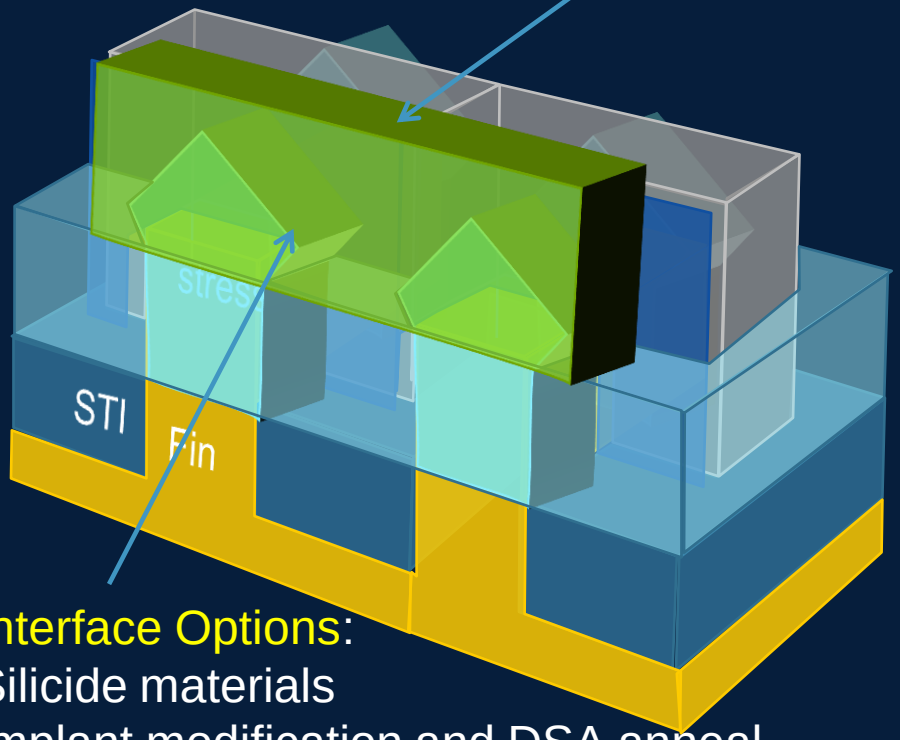
Tuning of WF metal by implant



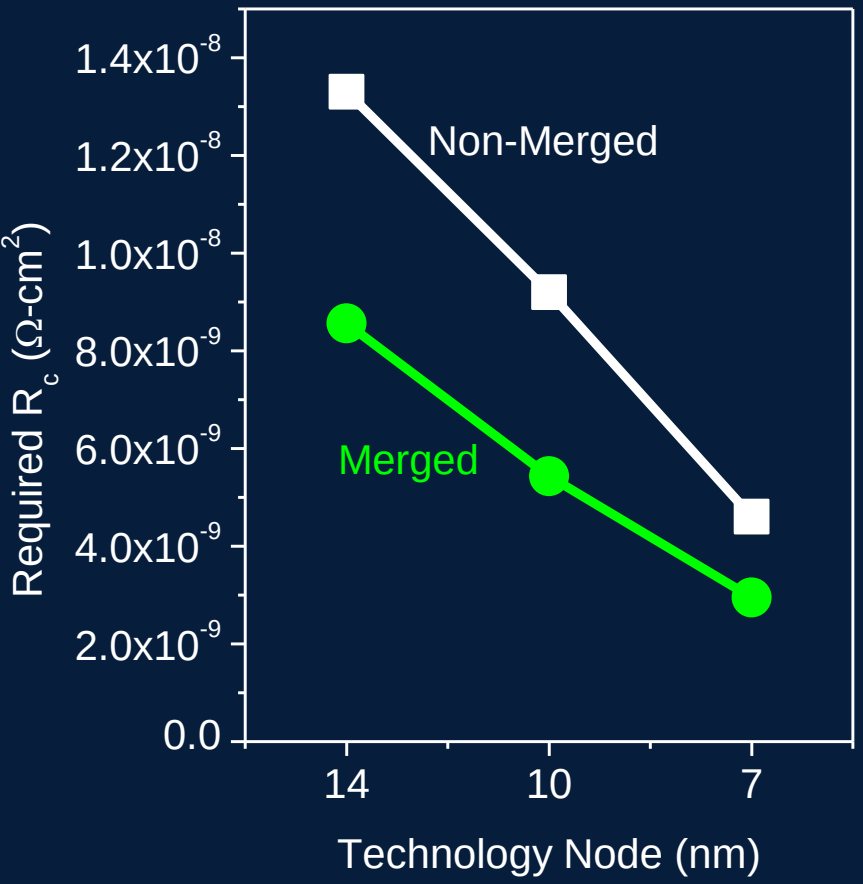
APPLIED MATERIALS

Silicide/Contact Challenge

Scalable contact fill

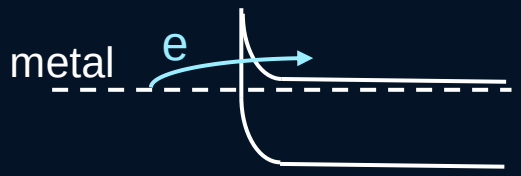


Interface Options:
Silicide materials
Implant modification and DSA anneal

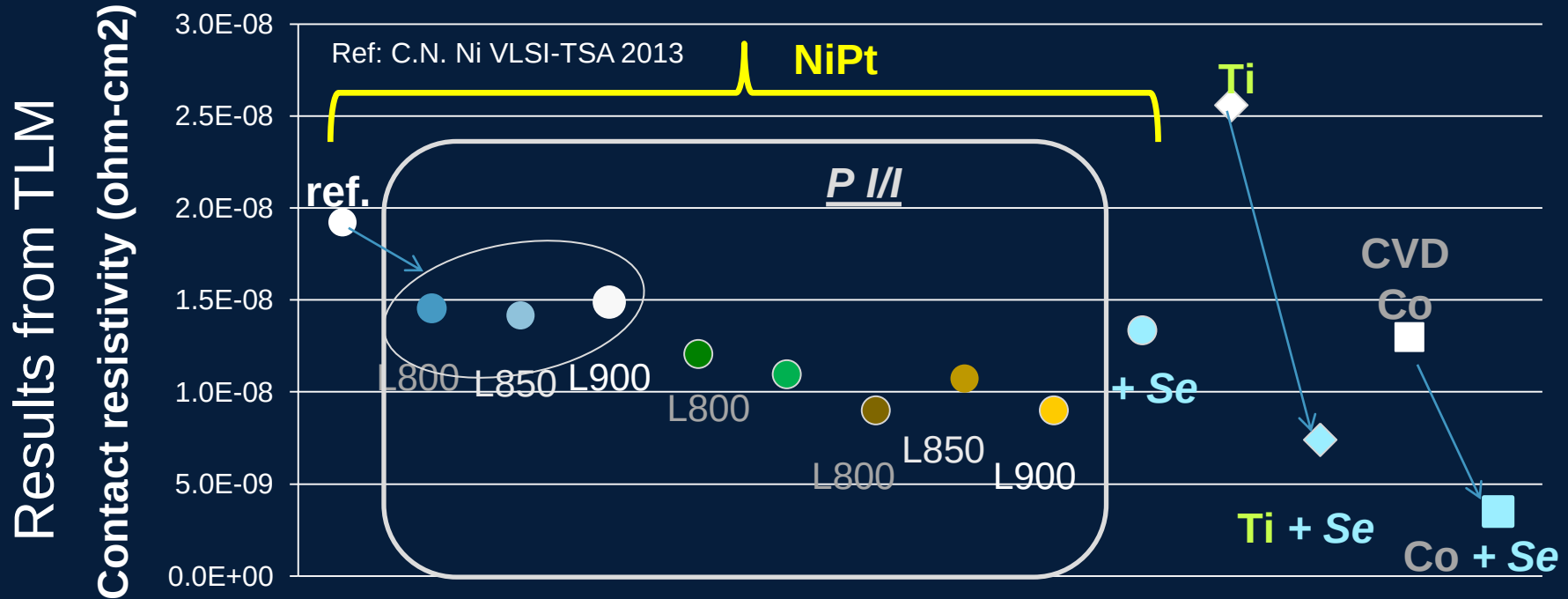


Must achieve R_c 5<10^{-9} Ω-cm² to meet resistance requirements

Silicide Rc Modification



Minimize schottky barrier
Limited by doping activation



Silicide Formation -> Implant -> DSA laser anneal for activation

Barrier reduction by P implant or Se implant with DSA activation

Summary

FinFET scaling requires precision control of materials

- CMP: precision through in-situ process control
- Dielectrics: composition tuning
- Junction: optimized activation
- Metal gate: multi Vt by metal gate composition and implant
- Metal gate: improved materials to control resistance at scaled CD
- Contact: optimized surface doping with implant + laser anneal

Acknowledgement: Raymond Hung, Aneesh Nainani, Chi-Nung Ni, Shiyu Sun, Bingxi Wood, Naomi Yoshida